ELECTRAC, INC.
140 Orangethorpe Way
ANAHEIM, CALIFORNIA

CHANNEL SEPARATION AND POLYPHASE DEMODULATION EQUIPMENT FOR A SS/FM TELEMETRY SYSTEM

FINAL ENGINEERING REPORT

PREPARED FOR: NASA, GEORGE C. MARSHALL SPACE FLIGHT CENTER
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BY: WARREN R. MUENGER
ELECTRAC, INC.
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I. ABSTRACT

This report contains theoretical analyses, circuit descriptions, design calculations, and measured performance data of the equipment supplied by Electrac, Inc. to George C. Marshall Space Flight Center under Contract Number NAS8-11651. This equipment provides channel separation and demodulation of 15 channels in a SS/FM telemetry system.

II. DISCUSSION

The equipment to be described was designed to overcome certain problems which arise in a suppressed-carrier single-sideband frequency-multiplexed telemetry system when pre-detection tape recording is employed. These problems become particularly severe in the case of vibration data covering the frequency range from 10 to 3000 cps. The primary difficulty is due to tape speed variations, or "flutter" which introduces frequency modulation of the entire subcarrier spectrum and thereby degrades the demodulation process of the lower baseband frequencies. In the specific equipment to be described, which utilizes subcarrier frequencies up to 71 kc., a typical tape recorder flutter of 1.2% peak-to-peak will introduce a carrier frequency uncertainty as much as 852 cps.

Another difficulty occurs when the subcarrier channels are closely spaced and channel separation is accomplished with bandpass filters. Because of the effective widening of the subcarrier spectrum caused by the tape recorder flutter, a filter which is designed without considering flutter will be too narrow to pass this widened spectrum. If the bandpass of the filter is widened sufficiently to pass all of the flutter-widened spectrum of its channel it will also pass a portion of the adjacent channels. In a system which has been designed with state-of-the-art bandpass filters, the additional requirements brought about by tape recorder flutter may be impossible to meet in a practical design.

Fortunately there is another technique which is capable of solving most tape-recorder-induced problems in a SS system. It requires only a carrier signal which is frequency-modulated by tape recorder flutter to the same degree as its associated sideband. This is the phasing approach in which two carrier signals differing in phase by 90° are applied to two demodulators, as shown in Figure 1-Block Diagram. The two demodulator outputs, which differ in phase by 90°, are operated upon by two phasing networks which have the property that their phase difference is 90° over the desired range of baseband frequencies. It is shown in Appendix A that this method can be used to select either the upper or lower sideband and that its equivalent selectivity as a filter may be made to far exceed that of any practical bandpass filter.

The phasing technique for generation and demodulation of single-sideband signals has been discussed at length in the literature and is used in practical voice communications systems in which the baseband is 300-3000 cps. The design of the phasing networks for this frequency range is quite simple and passive RC networks are commercially available for this purpose. In the case of vibration signals extending from 10 to 3000 cps the network design is not so simple, particularly if a passive network is contemplated. The procedures for determining the required phasing network response have been published but the synthesis problem for passive networks is enormously difficult when very small phase errors over a wide frequency range are to be realized.

We have bypassed the synthesis problem through the use of cascaded RC phase-shift networks which are separated by isolation amplifiers. This technique permits each term in the polynominal expression for the network response to be associated with its corresponding network section independently of the other sections. The synthesis procedure then becomes relatively simple since all component values can be computed directly from the polynominal terms.

Although the contractual requirements were for a set of "breadboard components" comprising the bandpass filters, the demodulators and the phasing networks as physically separate items, the system performance specifications are such that we could not be sure of attaining optimum performance except in an integrated package. We have therefore supplied the equipment as a set of 15 self-contained channels which require only external power and carrier sources. Figure 1 shows the functional block diagram for each channel.

It must be understood that the performance of this equipment depends primarily on four factors:

(a) The phase errors in the phasing networks. These errors are due to the 0.2° phase error ripple which is inherent in the network design plus another 0.2° which is allocated to component tolerances.

(b) The amplitude balance between the two halves of the phasing network. An amplitude adjustment has been provided which has been set for minimum undesired sideband output at about 300 cps. Because of component tolerances, this adjustment is not necessarily optimum across the entire 3000 cps band and amplitude unbalances on the order of 0.2% can be expected.

(c) Phase errors between the two carrier signals. We have made all of our measurements using a carrier generator in which the phase error is held to 0.1°.

(d) Harmonic and intermodulation distortion in the demodulators and phasing network amplifiers. Our measurements indicate that this distortion does not exceed 0.1% and might be considerably less.

III. CHANNEL SEPARATION FILTERS

Although the phasing networks alone are capable of providing the specified overall performance, we have included a bandpass filter in each channel which serves primarily to reduce the maximum input signal which the demodulators must accomodate. For this purpose a 3-pole design was determined to be adequate. Our design for these filters was based on 0.1 db ripple across the pass band including the spectrum widening due to tape recorder flutter. The measured response for the Channel 15 filter, which is typical of the other channels, is shown in Figure 2. The required inductor Q's are quite high (about 300) and it was necessary to use a tapped configuration to permit impedance transformation to the actual inductance values having the highest possible Q.

The inductors use adjustable ferrite pot cores and the capacitors are silver mica units which were selected to 1% tolerances. A table of filter design parameters is given in Appendix B. All filters were designed for 10,000 ohms input resistance and are driven directly from the composite input signal.

IV. DEMODULATOR DRIVER AMPLIFIER

The necessity for a driver amplifier for the demodulators arises from the fact that the signal input, being common to both demodulators, provides a potential source of carrier signal leak between the demodulators unless the signal source impedance is very low. The demodulator driver amplifier, shown in Figure 9, provides unity voltage gain but converts the 10,000 ohm bandpass filter impedance to an output impedance of 3 ohms to drive the demodulators. The demodulator driver amplifiers are identical except for Channels 1 and 2 which require balanced outputs. For these channels only, the demodulator driver consists of two amplifiers of the type used in the phasing networks, with one of these amplifiers providing the phase-inverted output. Referring to Figure 9, Q_1 is a wide-band common-emitter voltage amplifier which drives the complementary emitter followers Q2 and Q3. Overall voltage feedback is provided by R7. R1 matches the output impedance of the bandpass filter. This amplifier is flat within 3 db from 20 cps to about 15 mc and consequently contributes negligible phase and amplitude distortion of the input signal. Physically, the amplifier is located adjacent to one of the demodulators.

V. POLYPHASE DEMODULATORS

The demodulators use two four-diode series-gate circuits with square-wave current drive. This circuit has excellent linearity and uses no transformers which might introduce undesired phase shifts. It is not critical with respect to diode matching and it provides double-balanced operation wherein the output contains no components at the carrier and signal frequencies. All of the demodulators are identical but only on Channels 1 and 2 are both signal inputs driven. For the other channels the demodulator outputs contain signal frequency components which may be easily filtered out in a low-pass filter at the channel output.

Referring to the schematic diagram, Figure 4, Q1 is driven into saturation by a square-wave carrier frequency input signal having 0 and +1 volt levels. Q1 output is a square-wave signal of 8 volt peak-to-peak amplitude which drives the phase splitters Q2 and Q3. Because of the series connection, nearly the same current flows through R7 and R8 to develop two drive signals of equal amplitudes and opposite polarities. Since the collector current of Q2 supplies both base and collector current for Q3 the output of Q3 will be slightly less than that of Q2 if resistors R7 and R8 are equal. To compensate for the slight difference in currents R7 is shunted for equal outputs. Both output signals are 8 volts peak-to-peak. These signals provide square-wave drive current to the diodes by virtue of the resistors R9, R10, R13, and R14. The diodes in each half of the demodulator conduct alternately to provide full-wave demodulation of balanced inputs on Channels 1 and 2. For the other channels, only the "In 1" terminal is used for half-wave demodulation. On these channels "In 2" terminal is grounded.

The resistors R11 and R12 are used, in conjunction with the low output impedance of the driver amplifier, to isolate the two demodulators in each channel with respect to carrier leak.

Functionally, the demodulator performs a trigonometric multiplication between the carrier and input signals and therefore its output contains the sum and difference components. No filtering is used in the demodulator or in the phasing network since two matched filters would be required for this purpose and their use might deteriorate the desired 90° phase relationship.

The load resistor for one of the demodulators is fixed at 2000 ohms while the other load resistor is adjustable to provide overall amplitude balance for the channel. This adjustment compensates for differences between the two demodulators and, to a lesser extent, for unequal gains in the two halves of the phase network.

The demodulator will accept input signals as high as 2.5 volts rms without saturating but, for low distortion, is best operated at a level of 0.5 volts or less. Using unselected diodes, the carrier frequency output is approximately -40 db with respect to a signal input of 0.5 volts.

VI. PHASING NETWORKS

The phasing network (Figure 5) consists of a pair of nearly identical cascades, each containing five all-pass phasing sections. The only difference between the two cascades is in the capacitance values. Figure 6a shows a simplified representation of a typical section.

The amplifiers are direct-coupled amplifiers having negligible phase shift below 10 kc and a voltage gain of about 10,000. Because of this high gain, the operational gain is determined almost exactly by the ratio of feedback resistor to the input resistor. Referring to Figure 6b, R1 and R2 are equal and the voltage gain is therefore unity from input to output, provided that the reactance of the capacitor is small compared to the input resistance of the next section, which is also equal to R1. For frequencies at which the reactance of C is large, the signal passes also through the second amplifier A2 which has a gain determined by the ratio of R4 to R3. This ratio (1.2) is selected to exactly compensate for the loss in signal voltage as the signal passes through R5. The phase shift from input to output is exactly 90° at the frequency at which the reactance of C is equal to the resistance of R5 in parallel with the input resistance of the next stage. Because of the high internal voltage gain of the amplifiers, and the feedback connection, their effective output impedance is very low (less than 1 ohm) and their input impedance is very nearly equal to R1 or R3, respectively. The computational errors introduced by the amplifiers do not exceed 0.1% which is less than the component tolerances.

The total required number of phasing sections was determined from Figure 7, which was prepared with the aid of Weaver's paper[1]. Although 9 sections would meet the specified performance requirements,

1. Weaver, Donald K. "Design of RC Wide-Band 90-Degree Phase-Difference Network", Proceedings of the IRE, April 1954.

there would be no margin for component tolerances and therefore 10 sections were selected. According to Figure 6, an undesired sideband rejection of 54 db could be realized for ten (10) sections with perfect components.

Allowing 0.2% tolerances for the critical components, (primarily C and R5) the expected rejection would be somewhat less than 54 db depending on how the individual tolerances happened to combine in the overall network. Based on our measurements on all 15 channels, the minimum rejection is about 52 db on the average. For all of the critical components we selected those within 0.25% of the design center value and used RN60C metal-film resistors and polystyrene capacitors, most of which were procured to our particular values. Polystyrene capacitors, although possessing an appreciable temperature coefficient, have the lowest dissipation factor obtainable at the frequencies of interest. Their temperature coefficient is relatively unimportant since it is the same for all sections of the network and any changes due to temperature will merely shift the overall response uniformly along the frequency axis without degrading the rejection ratio.

For the smaller capacitor values, we found it more economical to use standard polystyrene units, which were padded with silver mica capacitors as necessary.

The amplifiers are all identical and are shown in Figure 8. The design of these amplifiers was based on the requirement for a voltage gain of at least 10,000 and practically zero phase shift to at least 10 kc. Due to normal variations between transistors it was necessary to individually equalize all amplifiers by means of a semi-adjustable capacitor C2 shunting the feedback resistor. Physically, this capacitor consists of a piece of twoconductor cable cut to proper length.

The schematic diagram shows Q1 and Q2 as a matched-pair differential input stage, Q3 and Q4 are a differential second stage, Q5 is a common-emitter amplifier and Q6 is an emitter-follower output stage. R3 and C1 provide a controlled gain roll-off at frequencies above 10 kc to permit stable operation with feedback. The overall frequency response with feedback is flat from DC to about 1 mc.

Figure 9 shows the calculated and measured phase difference of the breadboard version. The calculated points are accurate to about 0.1% due to slide-rule errors. The measured points were determined with the aid of an Ad-Yu 405H Phasemeter which was initially calibrated at 90° using our carrier frequency synthesizer. Figure 10 shows the calculated undesired sideband rejection for the breadboard network which is subject to additional slide-rule errors. The measured results show that the performance actually achieved is very close to the theoretical limits and that our test equipment and slide-rule computations were not quite adequate to fully assess the actual performance of the breadboard version. In testing the production units, we did not attempt to measure the phase difference of the networks but, instead, measured the overall sideband rejection. These measurements (see Appendix C) were also made at the limits of our test equipment. These measurements were made using an external 3 kc low-pass filter.

VII. DESCRIPTION OF EQUIPMENT

In our design of this equipment we attempted to go beyond what is usually classified as a "breadboard" and we believe that the final configuration could quite easily be modified and repackaged as a production item. All components are mounted on two